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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/502,445	09/07/2004	Axel Hulsmann	08788.0036USWO	5325

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MERCHANT & GOULD PC
P.O. BOX 2903
MINNEAPOLIS, MN 55402-0903

EXAMINER	
ARENA, ANDREW OWENS	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/502,445	HULSMANN, AXEL	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action (dated 02/21/2006).

Claims 1, 3, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hill (US 6,028,348) in view of Sovero (US 5,378,922).

Re claim 1, Hill discloses (Fig 7) an integrated circuit arrangement (col 8 ln 16-18) on the basis of III/V semiconductors (col 3 ln 22), comprising at least one active component (770; col 8 ln 17) and a multilayer configuration of wiring levels (414, 460, 704, 706, 708; col 7 ln 65, col 8 ln 5, 8) characterized in that:

a metallization layer comprising a metal contact (414; col 4 ln 27) of the at least one active component is formed to be a lower one of the wiring levels (414 is a wiring level: Fig 4L, also 4M), and that

said lower one of the wiring levels is deposited directly on top of a subcollector layer without a passivation layer (directly) underneath the lower wiring level.

Hill differs from the claimed invention only in not disclosing said lower wiring level connects the at least one active component with at least one passive component.

Sovero discloses (Fig 2) an integrated circuit arrangement on the basis of III/V semiconductors (col 2 ln 41) wherein a metallization layer (E) comprising a metal contact of an active component (14; col 3 ln 23, ln 29) formed to be a lower one of the

wiring levels, and said lower one of the wiring levels (E) connects the at least one active component (14) with at least one passive component (16; Fig 2: E; col 2 ln 50-51).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Hill in view of Sovero such that said lower wiring level connects the at least one active component with at least one passive component; at least for the desired device function (Sovero: col 2 ln 61-64).

Re claim 3, Hill discloses (Fig 7) an electric resistor (702) is formed in a wiring level (704, 706) by means of an interruption (702) in the metallization layer.

Hill differs from the claimed invention in not disclosing said wiring level is the lower wiring level and in not disclosing no additional resistive material is placed in the interruption in the metallization layer.

Sovero discloses (Fig 2) an electric resistor (16; col 3 ln 34) is formed in the lower wiring level (E+CE; col 3 ln 29) by means of an interruption in the metallization layer, and that no additional resistive material is placed in the interruption in the metallization layer (col 3 ln 34-36).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Hill in view of Sovero such that an electric resistor is formed in the lower wiring level (directly on the subcollector layer) and that no additional resistive material is placed in the interruption in the metallization layer; at least to provide several advantages (Sovero: col 3 ln 58-66).

Re claim 9, Hill discloses (Fig 7) the at least one active semiconductor component (770) is a transistor (col 8 ln 17, col 3 ln 14-15) and

Hill as modified by Sovero discloses a metal contact of the collector of the transistor is formed by means of the metallization layer.

Claims 2, 4-8, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hill in view of Sovero as applied to claim 1 above, and further in view of Ko (US 6,696,538).

Re claim 2, Hill discloses (Fig 7) a passivation layer (455; col 4 ln 41) made of a material which has a small relative dielectric constant εr1 (small relative has been interpreted to encompass Hill 455) is applied on the metallization layer of the at least one active component (455 is on 414).

Hill differs from the claimed invention only in not disclosing said small relative dielectric constant obeys the equation $\varepsilon r1 < 3$.

Ko teaches a dielectric constant less than three (col 1 ln 45, ln 60, col 2 ln 11) is preferable in a device such as that of Hill (MMIC; col 6 ln 11).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that the small relative dielectric constant of Hill obey the equation $\varepsilon r1 < 3$, as taught by Ko; at least to decrease crosstalk noise (col 1 ln 45-47).

Re claim 4, Hill discloses a central wiring level (702+704+706; col 7 ln 60-65) is disposed above the passivation layer (455) and covered by another passivation layer (755; col 8 ln 5-6) made of a material (SiN) which has a mean relative dielectric constant εr2 that obeys the equation $\varepsilon r2 > \varepsilon r1$ (it is known that $\varepsilon r(SiN) > 3$).

Re claim 5, Hill discloses (Fig 7) an upper wiring level (708, 476; col 8 ln 8, col 5 ln 12) is disposed above the central passivation layer.

Re claim 6, Hill discloses (Fig 7) a capacitive component (706+755+708; col 7 ln 65, col 8 ln 5-9) is formed by means of a section (706) of the central wiring level and a section (708) of the upper wiring level.

Re claim 7, the product-by-process limitation "the upper wiring level is formed by galvanic deposition of metal" has not been given patentable weight. See MPEP § 2113.

Re claim 8, Hill discloses (Fig 7) the upper wiring level is constructed at least partly by air bridge technology (476; col 5 ln 10-13).

Re claim 9, Hill discloses (Fig 7) the at least one active semiconductor component (770) is a transistor (col 8 ln 17, col 3 ln 14-15) and

Hill as modified by Sovero discloses a metal contact of the collector of the transistor is formed by means of the metallization layer.

Re claim 12, Hill discloses the mean relative dielectric constant obeys the equation $\varepsilon r2 \approx 7$ (col 8 ln 6; SiN is known to have a dielectric constant of about 7).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hill, Sovero and Ko as applied to claim 5 above, and further in view of Baba (US 6,853,054).

Re claim 10, Hill differs from the claimed invention only in not disclosing at least one microstrip conductor.

Baba discloses (Fig 4) at least one microstrip conductor (16+18 and 20+18; col 5 ln 10, ln 15-17) formed by means of the various wiring levels (Baba uses the terms

transmission line and microstrip interchangeably for a wiring layer adjacent to a grounded layer: col 1 ln 38-40, ln 67, col 2 ln 1, col 4 ln 24-29).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Hill in view of Baba such that ate least one microstrip conductor is formed by means of the lower, the central, and the upper wiring levels; at least for stabilizing transmission characteristics (Baba: col 5 ln 17-18).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hill, Sovero and Ko as applied to claim 5 above, and further in view of Shimamoto (US 6,683,260).

Re claim 11, Hill differs from the claimed invention only in not disclosing a waveguide.

Shimamoto discloses (Fig 1A) a waveguide (3a&3b+5b; col 6 ln 49-50) formed in the wiring levels.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Hill in view of Shimamoto such that waveguides are formed on the lower and/or the central and/or the upper wiring levels; at least for excellent transmission characteristics (Shimamoto: col 8 ln 45-48).

Response to Arguments

Applicant's arguments filed 09/13/2006 have been fully considered but they are not persuasive.

Applicant's arguments filed 09/13/2006 "incorporates by reference the remarks with respect to [Hill] in the Second Response filed May 22, 2006". The application file does not contain a response dated May 22, 2006, but does contain a response dated May 24, 2006. This appears to be the above-referenced response. In reply, examiner repeats the Response to Arguments made in the Non-Final Rejection dated 6/14/2006: "Applicant's arguments filed 05/24/2006 have been considered but are moot in view of the new grounds of rejection."

Applicant's alleged features of Sovero not mentioned therein, but asserted to "must be" present are not germane to the combination made by the examiner for at least two major reasons.

First, the contentious feature of a wiring level "deposited directly on top of a subcollector layer..." is already present in Hill, rendering any discussion thereof in Sovero moot. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See MPEP § 2145(IV).

Second, applicant's alleged features of Sovero (even if accurate) would only be present in the embodiment where the ballasting resistor is connected to the emitter. However, the rejection relies upon the embodiment of Sovero, where the ballasting resistor is connected to the collector (col 2 ln 50-52).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is 571-272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on 571- 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Andrew O Arena
26 November 2006

Douglas W. Owens 11/27/06
DOUGLAS W. OWENS
PRIMARY EXAMINER